E101

EtherNet/IP, CC-Link SPI Module

Product Specification

Version	Issue date	Changes	Remark
0.1	2018/01/08	Initial Version	
1.0	2024/11/28	Update SPI timing	

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E101 EtherNet/IP, CC-Link SPI Module

1. Introduction

EtherNet/IP is an industrial network protocol that adapts the Common Industrial Protocol to standard Ethernet. EtherNet/IP is one of the leading industrial protocols in the United States and is widely used in a range of industries including factory, hybrid and process. The EtherNet/IP and CIP technologies are managed by ODVA, Inc., a global trade and standards development organization founded in 1995 with over 300 corporate members.

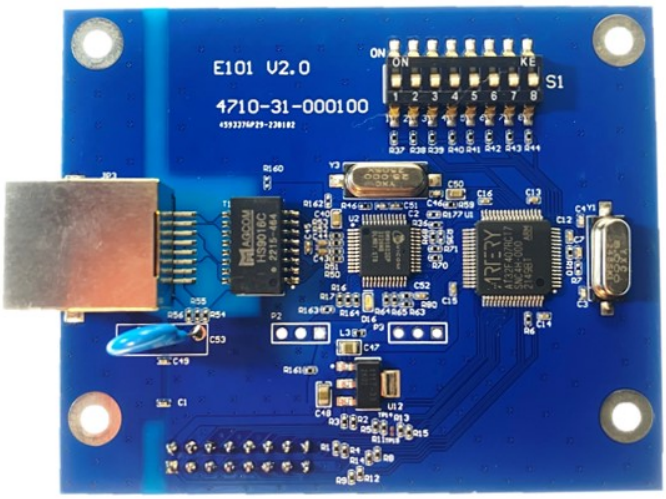
CC-Link (Control and Communication Link) is an open industrial network protocol designed for automation and control systems. Developed by the CC-Link Partner Association (CLPA), it facilitates communication between a wide range of devices, such as programmable logic controllers (PLCs), sensors, actuators, and human-machine interfaces (HMIs).

By using a proprietary SPI interface, E101 is a general purpose device adaptor for connecting device to an EtherNet/IP or CC-Link bus network.

Major Applications :

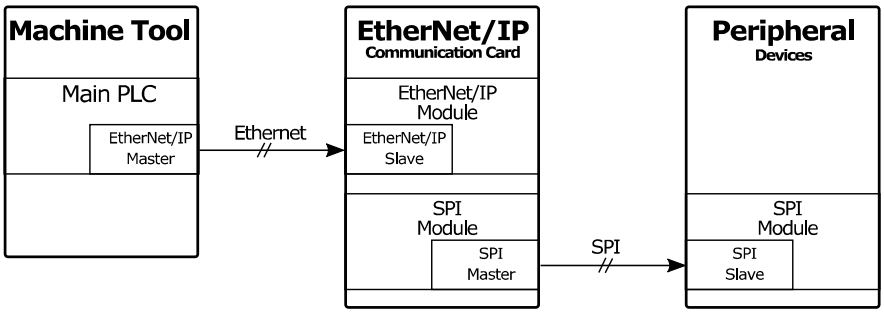
- Remote IO
- HMI
- Sensor
- Industrial automation

Product Picture :



2. Specification

2.1 System block diagram



2.2 Key specifications

Item	Specification
Power source	5V DC ±10%, Supplied by Device
Current consumption	< 300mA
SPI interface voltage level	5V TTL, 5V is logic 1, 0V is logic 0
Operating condition	Temperature -10℃～55℃ Humidity 20 ~ 85% RH
Data update rate	< 2ms for all DI and DO data

2.3 SPI interface

E101 board communicate device with a dual row 16P 2.54mm header and socker. E101 board is male header and device is female socket. The pin definition of 16P header is :

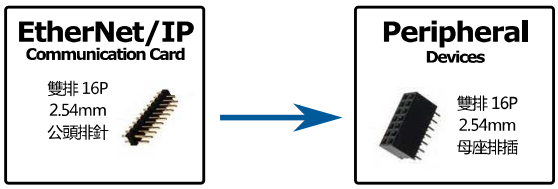
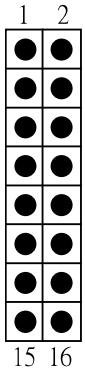


Figure 1 E101 and Device connection interface



16P Header pin definition

PIN	SYNBOL	Description
1	+5V	5V DC power, supplied from Device
2	+5V	5V DC power, supplied from Device
3	MOSI	Master Out-Slave In, E101 → Device
4	MISO	Master In-Slave Out, Device → E101
5	SCK	Clock, generated by E101
6	CS	Slave Select，E101 → Device，active low
7	RTS	Request to send，E101 → Device，E101 is ready to send data
8	CTS	Clear to send，Device → E101，Device is ready to send data
9		Reserved I/O 1
10		Reserved I/O 2
11		Reserved I/O 3
12		Reserved I/O 4
13	DS1	Data select 1
14	DS2	Data select 2
15	0V	Ground
16	0V	Ground

1. E101 is powered by Device through PIN1 and PIN. The voltage is 5V DC. PIN15 and PIN16 is ground.
2. PIN3 ~ PIN6 are SPI interface signals.
3. PIN7 ~ PIN8 are SPI flow control signal.
4. PIN9 ~ PIN12 are reserve for future expansion.
5. PIN13 ~ PIN14 are device DIO quantity selection. Whenever E101 power up, it will read the value of these two signals to determine device's quantity of DIO.

DS2	DS1	Number of I/O
1	1	16DI/16DO，16 Digital Input & 16 Digital Output
1	0	32DI/32DO，32 Digital Input & 32 Digital Output
0	1	64DI/64DO，64 Digital Input & 64 Digital Output
0	0	96DI/96DO，96 Digital Input & 96 Digital Output

6. DS1 and DS2 are internally pull up. When floating, the logic is 1.

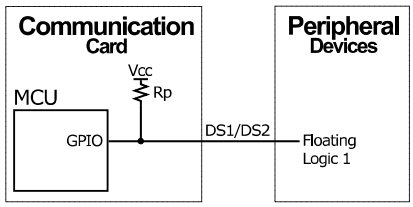


Figure 2 DS1/DS2 floating

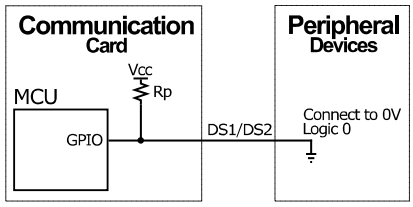
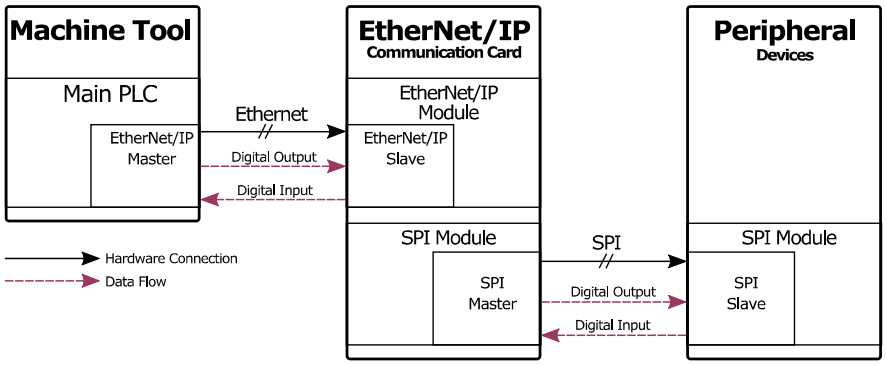


Figure 3 DS1/DS2 connecting to 0V

2.4 E101 IP address setting

The E101 IP address is 192.168.100.XXX and the XXX : 0~255 is set by DIP switch. For enabling a new setting, the E101 must be power off and on once.



2.5 SPI communication protocol

There are four SPI clock modes :

SPI MODE	SCK Status	Shift Operation SCK Edge	Capture Operation SCK Edge
Mode 0	Active High	Falling	Rising
Mode 1	Active High	Rising	Falling
Mode 2	Active Low	Rising	Falling
Mode 3	Active Low	Falling	Rising

Figure 4 SPI clock mode

E101 uses clock Mode 0. This means that SCK rising edge trigger the data capture and store the data during falling edge.

SPI data is MSB(Most Significant Bit) first.

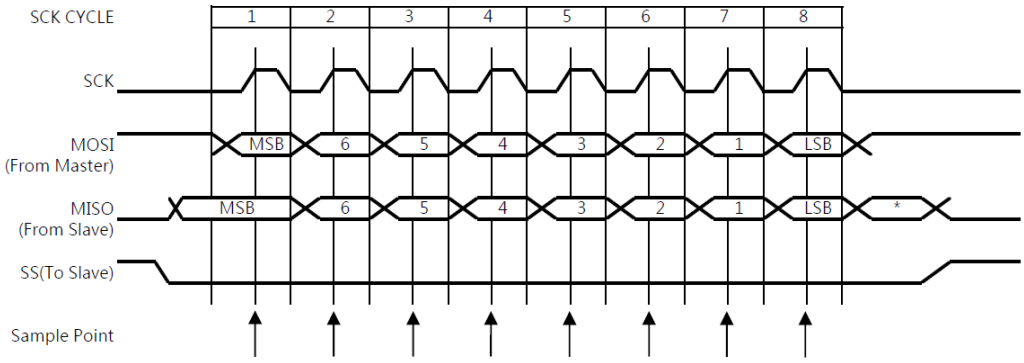


Figure 5 SPI timing diagram for mode 0

2.5.1 SPI packet format

The packet format used by E101 in communication with Device through SPI interface is listed in figure 6 below.

BYTE	01	02	03	04	05 ~ 22	23
SYMBOL	B01	B02	B03	B04	B05 ~ B22	B23
FUNCTION	START BYTE 1	START BYTE 2	LENGTH	CMD	DATA PAYLOAD	CHECKSUM
VALUE	0x55	0xAA	0x17	CMD	PAYLOAD	CHECKSUM

Figure 6 SPI packet format

The packet length is fixed 23bytes

1. The beginning 2 bytes (B01,B02) are fixed (0x55,0xAA)
2. B03 is the packet length, now it is fixed 0x17(23 bytes)
3. B04 is command byte
4. B05~B22 are data bytes
5. B23is checksum byte

The definition of command byte is listed in Figure 7 :

CMD	Function	Data Description
0x01	Digital Input, DI	18 bytes DI data, 144 DI maximum
0x02	Digital Output, DO	18 bytes DO data, 144 DO maximum

Figure 7 SPI packet command byte definition

The data bytes B05~B22 are defined according to the DIP switch DS1/DS2 status during power on. The unused bytes are filled with 0.

For example, DS1/DS2 = 1/1, E101 and Device determine the I/O number is 16DI/16DO, then the packet format is shown as figure 8 and figure 9

BYTE	01	02	03	04	05	06	07	08	09	10	11	12
SYMBOL	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12
VALUE	0x55	0xAA	0x17	0x01	DI01	DI02	0	0	0	0	0	0
BYTE	13	14	15	16	17	18	19	20	21	22	23	
SYMBOL	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	
VALUE	0	0	0	0	0	0	0	0	0	0	SUM	

Figure 8 SPI packet example 1 (16DI)

BYTE	01	02	03	04	05	06	07	08	09	10	11	12
SYMBOL	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12
VALUE	0x55	0xAA	0x17	0x02	DO01	DO02	0	0	0	0	0	0
BYTE	13	14	15	16	17	18	19	20	21	22	23	
SYMBOL	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	
VALUE	0	0	0	0	0	0	0	0	0	0	SUM	

Figure 9 SPI packet example 2 (16DO)

In condition of DS1/DS2 = 0/0, the E101 and Device determine I/O number is 96DI/96DO, then the packet format is shown as figure 10 and figure 11.

BYTE	01	02	03	04	05	06	07	08	09	10	11	12
SYMBOL	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12
VALUE	0x55	0xAA	0x17	0x01	DI01	DI02	DI03	DI04	DI05	DI06	DI07	DI08
BYTE	13	14	15	16	17	18	19	20	21	22	23	
SYMBOL	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	
VALUE	DI09	DI10	DI11	DI12	0	0	0	0	0	0	SUM	

Figure 10 SPI packet example 3 (96DI)

BYTE	01	02	03	04	05	06	07	08	09	10	11	12
SYMBOL	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12
VALUE	0x55	0xAA	0x17	0x02	DO01	DO02	DO03	DO04	DO05	DO06	DO07	DO08
BYTE	13	14	15	16	17	18	19	20	21	22	23	
SYMBOL	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	
VALUE	DO09	DO10	DO11	DO12	0	0	0	0	0	0	SUM	

Figure 11 SPI packet format 4 (96DO)

The last byte B23 is used for error checking. The checksum is calculated by formula below :

$$\mathrm{NOT}\left(\sum_{n=1}^{22} \mathrm{Bn}\right) + 1$$

It is the 2'compliment of B01~B22 sum.

2.5.2 SPI flow control

Because E101 is SPI Master and Device is Slave, the device may not be ready for sending when E101 is ready for sending data. The RTS/CTS signals are used to make sure Device is ready before E101 launch the SPI communication.

Whenever E101 is ready for sending data, E101 must set RTS to logic 1, this inform device that E101 is ready. Whenever Device receive RST=1, Device should set CTS to 1 if Device is ready for sending data. Once E101 receive CTS=1, it will launch the SPI communication. Because both are ready for sending data, the communication can be completed reliably.

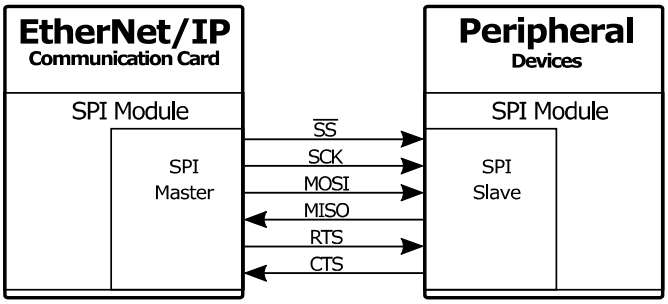


Figure 12 SPI communication diagram

2.6 *Detail dimension*

The DWG file of dimension is available under request.